AMENDMENTS TO THE SPECIFICATION:

Page 7:

Please substitute the following paragraph for the paragraph beginning at line 11:

Figs. [[4]] 4(a) and 4(b) illustrate the relationship among voltages applied to different films in the memory cell of Fig. 3.

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Please substitute the following paragraph for the paragraph beginning at line 10:

Fig. 1 is a block diagram of a flash memory, which is the preferred embodiment of the invention; Fig. 2 illustrates the configuration of an erase voltage switching circuit provided in the flash memory of Fig. 1; Fig. 3 illustrates the configuration of a memory cell provided in the flash memory of Fig. 1; Figs. [[4]] 4(a) and 4(b) illustrate the relationship among voltages applied to different films in the memory cell of Fig. 3; Fig. 5 illustrates the erase distribution in the memory cell of Fig. 3; Fig. 6 is a flow chart of the erasion sequence of memory cells in the flash memory of Fig. 1; Fig. 7 through Fig. 9 illustrate one example of soft erase voltage setting in the erase operation for the memory cell of Fig. 3; Fig.

10 through Fig. 13 illustrate another example of soft erase voltage setting in the erase operation for the memory cell of Fig. 3; Fig. 14 illustrates the relationship among voltages at the time of erasing data in a memory cell studied by the present inventors as a comparative example; Fig. 15 illustrates the erasion characteristics of the memory cell of Fig. 14 including fluctuations; Fig. 16 illustrates the threshold voltage in the memory cell of Fig. 14; Fig. 17 illustrates the floating gate voltage at the time of erasion in the memory cell of Fig. 14; Fig. 18 illustrates the voltage between the control gate and the floating gate of the memory cell of Fig. 14; Fig. 19 illustrates comparison of the loci of the threshold voltage of a memory cell wherein the soft erase voltage is divided by different numbers in the embodiment of the invention; Fig. 20 illustrates comparison of the loci of the floating gate voltage of a memory cell wherein the soft erase voltage is divided by different numbers at the time of erasion in the embodiment of the invention; and Fig. 21 shows test data of comparison of retention characteristics in a state of being let stand at high temperature between erasion of data in the memory cell studied by the present inventors for comparison and erasion of data in the memory cell with a bisected soft erase voltage in this embodiment of the invention.